PVP 12

Code: EM3T6, EE3T4

II B.Tech - I Semester – Regular Examinations – December 2014

SWITCHING THEORY AND LOGIC DESIGN
(Common for ECM, EEE)

Duration: 3 hours Marks: 5x14=70

Answer any FIVE questions. All questions carry equal marks

1 a) Convert the decimal number 508.75 to base 7, 8 and 12. 7 M

b) Represent the decimal number 7258 in 7 M
i) BCD code ii) excess-3 code
iii)2421 code iv) 6311 code

2 a) Simplify the following Boolean expressions to a minimum number of literals? 7 M

i) $xy+x\bar{y}$ ii) $(x+y)(x+\bar{y})$

iii) $xyz+\bar{x}y+xy\bar{z}$ iv) $(\overline{A+B})(\overline{\bar{A}+\bar{B}})$

b) Find the dual and compliment of the following expressions 7 M

i) $x\bar{y}+\bar{x}y$ ii)$(A\bar{B}+C)\bar{D}+E$

iii) $(x+\bar{y}+z)(\bar{x}+\bar{z})(x+y)$

3 For the given function 14 M

F(A, B, C, D, E) =

Σ m (0,1, 2, 3, 4, 5, 9, 10, 16, 17, 18, 19, 20, 22, 25, 26)

+ Σ d (7, 11, 12, 13, 15, 23, 27, 28, 29, 30)

Obtain minimal sop expression using K-Map.

4 a) Design a 32:1 Multiplexer using two 16:1 and 2:1Multiplexers. 8 M

b) Write short notes on look-ahead adder circuit. 6 M

5 a) Implement the following Boolean functions with a PLA. 8 M

i) F (x,y,z) = Σ (0,1,2,4) ii) F (x,y,z) = Σ (0,5,6,7)

b) Implement Full adder circuit using ROM. 6 M

6 a) Design a modulo-9 counter using T flip-flops with preset and clear inputs. 8 M

b) Compare synchronous & Asynchronous circuits. 6 M

7 a) Explain the salient features of the finite state machine? 7 M

b) Draw the state diagrams of a sequence detector which can detect 011. 7 M

8 a) Explain briefly about the hazards and hazard free realizations? 8 M

b) Explain about Races in asynchronous sequential logic circuit. 6 M